AMENDMENTS TO THE CLAIMS

Please cancel claims 1-20 and 30-32 without prejudice, please add new claims 33-47, and please amend claims 21-22 and 24-28 as follows:

1 – 20 (Currently Cancelled)

21. (Currently Amended) A method ~~for fabricating a transistor~~ comprising:

forming an insulated gate;

forming insulating spacers adjacent to sidewalls of the gate;

forming extension regions after forming the insulating spacers; and

forming a source and a drain.

22. (Currently Amended) A transistor ~~fabricated~~ formed by the method of claim 21.

23. (Original) The method of claim 21, wherein forming the extension regions after forming the insulating spacers comprises doping regions of a substrate that are aligned with outer edges of the previously formed insulating spacers.

24. (Currently Amended) The method of claim 21, wherein forming the insulating spacers comprises:

depositing an insulating layer over at least a portion of a substrate containing the insulated gate, over a top of the insulated gate, and over sidewalls of the insulated gate; and

removing portions of the deposited layer from over the portion of the substrate and from over the top of the insulated gate while leaving portions of the layer over the sidewalls of the insulated gate.

25. (Currently Amended) The method of claim 24: (i) wherein depositing includes depositing the oxide of silicon on the sidewalls of the insulated gate by a chemical vapor deposition; and (ii) wherein removing includes removing the portions ~~of the oxide of silicon~~ by an anisotropic etch.

26. (Currently Amended) A transistor ~~fabricated~~ formed by the method of claim 25.

27. (Currently Amended) The method of claim 21, wherein forming the insulating spacers comprises:

growing an insulating layer over at least a portion of a substrate containing the insulated gate, over a top of the insulated gate, and over sidewalls of the insulated gate; and

removing portions of the deposited layer from over the portion of the substrate and from over the top of the insulated gate while leaving portions of the layer over the sidewalls of the insulated gate.

28. (Currently Amended) The method of claim 27: (i) wherein growing includes growing an oxide of silicon on the sidewalls of the gate by thermal oxidation of silicon of the sidewalls of the insulated gate; and (ii) wherein removing includes removing the portions ~~of the oxide of silicon~~ by an anisotropic etch.

29. (Original) The method of claim 21, wherein forming extension regions after forming the insulating spacers comprises forming doped extension regions by using the previously formed insulating spacers as alignment masks.

30 – 32 (Currently Cancelled)

33. (New) The method of claim 21, wherein forming the insulating spacers adjacent to the sidewalls of the gate comprises forming insulating spacers that abut the sidewalls of the gate.

34. (New) The method of claim 21, wherein forming the insulating spacers comprises forming an insulating spacer containing an oxide of silicon.

35. (New) The method of claim 34, wherein forming the insulating spacers comprises forming an insulating spacer containing silicon dioxide.

36. (New) The method of claim 21, wherein forming the insulating spacers comprises forming insulating spacers having a thickness in a range between 10-200 Angstroms.

37. (New) The method of claim 36, wherein forming the insulating spacers comprises forming insulating spacers having a thickness in a range between 20-100 Angstroms.

38. (New) The method of claim 21, wherein forming the insulating spacers comprises forming insulating spacers having a thickness that is sufficient to reduce a capacitance associated with the gate and an extension region to less than approximately 0.4fF/um.

39. (New) The method of claim 21, further comprising removing the insulating spacers after forming the extension regions.

40. (New) The method of claim 39, wherein removing the insulating spacers comprises performing a wet etch.

41. (New) A method comprising:

forming insulating spacers adjacent to sidewalls of an insulated gate by:

(i) depositing an insulating layer containing an oxide of silicon and having a thickness in a range between 10-200 Angstroms over at least a portion of a substrate containing the insulated gate, over a top of the insulated gate, and over sidewalls of the insulated gate; and

(ii) removing portions of the deposited layer from over the portion of the substrate and from over the top of the insulated gate while leaving portions of the layer over the sidewalls of the insulated gate;

forming extension regions after forming the insulating spacers by doping regions of the substrate that are aligned with outer edges of the insulating spacers; and

forming a source and a drain by ion implantation.

42. (New) The method of claim 41: (i) wherein depositing includes depositing the oxide of silicon on the sidewalls of the insulated gate by a chemical vapor deposition; and (ii) wherein removing includes removing the oxide of silicon by an anisotropic etch.

43. (New) The method of claim 41, wherein forming the insulating spacers comprises depositing the oxide of silicon on the sidewalls of the gate.

44. (New) The method of claim 41, wherein depositing the insulating layer containing the oxide of silicon comprises depositing an insulating layer containing silicon dioxide.

45. (New) The method of claim 41, wherein depositing the insulating layer having the thickness in the range between 10-200 Angstroms comprises depositing an insulating layer having a thickness in a range between 20-100 Angstroms.

46. (New) The method of claim 41, further comprising removing the insulating spacers after forming the extension regions by performing a wet etch.

47. (New) A transistor formed by the method of claim 41.